BOHR International Journal of Intelligent Instrumentation and Computing
2021, Vol. 1, No. 1, pp. 1–4

https://doi.org/10.54646/bijiiac.001
www.bohrpub.com

An Efficient Design of 16 Bit MAC Unit using Vedic Mathematics

N. Manoj Kumar, G. Saravanan, D. Shyam Ganesh and S. Kanimozi

Department of Electronics and Communication Engineering, Vel Tech High Tech Dr. Rangarajan Dr. Sakunthala Engineering College, Avadi, Chennai, Tamil Nadu

Abstract. Duplicate and Accumulate (MAC) is one of the central practices utilized absolutely in signal-controlling and different applications. The multiplier is the major piece of Digital Signal Processors (DSPs). Its cutoff spins around power, LUT use, and surrender pick the presence of a DSP. In like way, there is a need to sort out the drive and give up fit multiplier. In this paper, a 16-digit MAC unit is proposed to utilize an 8-cycle Vedic multiplier and pass on a save snake. A relationship with the current 8-cycle Vedic multiplier utilizing Square-Root (SQR) Carry-select snake (CSLA) is introduced. It is isolated and a standard pack multiplier. The whole technique is done in Verilog HDL. Blend and redirections were finished utilizing Xilinx InDesign Suite 14.5. The proposed game plan accomplishes fundamental improvement in region and suspension. In like manner, an abatement in power around 9.5% is refined.

Keywords: MAC unit, Vedic mathematics, Carry-save adder, Verilog HDL, Look-up Table.

Introduction

LOW fundamental moves an undeniable occupation in the current latest things of VLSI. Force dispersal has become a colossal improvement objective because of the all-inclusive interest in low-power advanced sign processors. There are various frameworks and expansion circuits used to accomplish low force in VLSI plans. In an "Advanced Signal Processor" (DSP), the reliably utilized activities are "augmentation and aggregate" (MAC), convolution, and "Lively Fourier Transforms" (FFT, and so forth The multiplier is viewed as a focal square for the above works out. Force use in a DSP extraordinarily relies on the MAC unit. Macintosh unit contains a multiplier, a snake for adding its halfway things, and an aggregator for dealing with the got results. So for improving the speed of the MAC unit, the speed of the multiplier ought to be improved. A pass-on save snake is utilized subsequently and out-of-date Vedic number shuffling is utilized for accomplishing reduces in power. This work underlines orchestrating a 16-digit MAC unit with an 8-cycle Vedic-multiplier utilizing urdhvatiryak (UT) thinking and uses a pass-on save snake for adding the halfway things. It is then separated and a typical show multiplier and a current 8-cycle Vedic-multiplier utilizing SQR-CSLA. As duplication is named as a generally utilized figuring development, the examination has dependably been wanting to plan quick multipliers either by showing overhauls in force, zone, or deferral. In a MAC arrangement proposed utilizing a streamlined multiplier, different cutoff points were settled for 8 bit, 16 bit, and 32 bit MAC units. The producers in [2] proposed a MAC utilizing Vedic sutras and finished in 90 nm advancement showing redesigns in circuit power, fundamental way postponement, and locale in 4 bit, 8 bit MAC units autonomously. Planning for organizing a 16 bit Vedic-multiplier utilizing urdhva tiryakbhyam (UT) with three specific adders has been done in and accomplished around a 32% decrease in combinational way delay separated from the past models.

Literature Survey

"Hybrid Multiplier-based Optimized MAC Unit", Dwivedi, Kavindra & Sharma Sharma, R. K. & Chunduri, Ajay

Any place there is a requirement for elite processing applications there is an obvious interest for an effective rapid multiplier. Augmentation takes the main time when contrasted with other number-crunching activities. Multipliers are the most fundamental squares in each elite registering design like Digital sign handling (DSP). Macintosh unit which comprises of Multiplier and Accumulator assumes a significant part to choose the exhibition

of any DSP block. The better presentation of the MAC unit satisfies the boundary of quick calculation and ongoing preparing capacities of a DSP. Throughout the long term, various thoughts have been proposed to improve the presentation and alleviate the over-the-top incomplete item term age during the traditional augmentation approach. In this paper, we have zeroed in on proposing the MAC design utilizing a coordinated Hybrid paired Multiplier and incorporated CLA viper organization. The coordinated multiplier is a mix of the Karatsuba calculation and Urdhva Triyagbhyamsutra from Vedic math. CLA viper network comprises of CLA and restrictive whole snake which assists with decreasing expansion time by performing equal expansion.

"Parallel Multiplier-accumulator Unit based on Vedic Mathematics", Jithin S, Prabhu E

In this paper, a compelling equivalent multiplier and gatherer (MAC) unit reliant on Vedic math is presented. Vedic science utilizes the Urdhva-tiryagbhyam sutra for the multiplier plan. The proposed MAC configuration overhauls the speed of movement while diminishing the doorway zone and power dispersing. We in like manner achieve an improved deferral with the help of the Vedic encoder followed by the departure of the finder stage by parallelizing the midway results dealing with the information. Such pipelining of the midway results, before the last snake, merges the aggregator stage with the fragmentary thing period of the multiplier. Further, the overall computation speed of the MAC unit is raised by the successful usage of higher-demand blowers in the consolidated inadequate thing pressing factor and gatherer (PPCA) designing. The region, timing, and power reports show that the fundamental path deferment of the proposed setup is by and largely decreased and it beats the current plans. We report level out the progress of 20–30% and 7–18% separately for the 4-cycle and 8-digit Vedic MAC units, with respect to their full-scale circuit power, essential way delay, and cell zone. The plan was mixed using a standard 90 nm CMOS library and executed on Altera's Cyclone II course of action FPGA.

"Design and Optimization of 16 × 16 Bit Multiplier Using Vedic Mathematics", S. N. Gadakh and A. K. Khade

Enlargement is a critical cutoff in the measure of changing tasks. Development-based activities, for example, duplicate and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), isolating are by and large utilized in signal managing applications. As duplication overwhelms the execution period of DSP structures, there is a need to create fast multipliers. Old Vedic mathematical longings the reaction fairly. In this paper, the chance of Urdhwa-Tiryagbhyam is utilized i.e., vertically and momentarily amplification to execute a 16 × 16 Bit Vedic multiplier, and improvement is made by utilizing the pass on saving adders. Secluding and past plans, the proposed configuration accomplishes a 33.26% reducing in combinational way delay. The Vedic multiplier proposed is executed in VHDL while joined and imitated utilizing Xilinx ISE Design Suite 14.5.

"Low Power High Speed 16 × 16 bit Multiplier using Vedic Mathematics", K. Bathija, R & S. Meena, R & Sarkar, S & Sahu, Rajesh

High-speed equivalent multipliers are one of the keys in RISCs (Reduced Instruction Set Computers), DSPs (Digital Signal Processors), and delineations gas pedals, and so on Arraymultiplier, Booth Multiplier, and Wallace Tree multipliers are a bit of the standard approaches used in the execution of combined multiplier which is sensible for VLSI execution. An essential mechanized multiplier (from now on insinuated as VedicMultiplier in short VM) plan subject to the Urdhva Tiryakbhyam (Vertically and Crosswise) Sutra of Vedic Mathematics is presented. An improved system for low-power and quick multiplier of two twofold numbers (16 cycles each) is made. A count is proposed and executed on 16 nm CMOS advancement. The arranged 16 × 16 piece multiplier disperses a power of 0.17 mW. The spread concedes period of the proposed configuration is 27.15 ns. These results are various redesigns overpower dispersals and concede declared in the composition for Vedic and Booth Multiplier.

"An Efficient Booth Multiplier Using Probabilistic Approach", M. V. Durga Pavan and Ramesh, S. R.

In VLSI Design, low force decrease is accomplished by primarily lessening the force. As of now, low-power plans are transcendent in VLSI because of numerous reasons. The fundamental center is to decrease the warmth in the gadget. From the essential numerical conditions of force, a decrease of force should be possible by either diminishing clock, diminishing voltage, or diminishing burden. The alternative of diminishing force should be possible by lessening voltage as timekeepers ought to be kept up for quicker frameworks. Force decrease should be possible at different levels like design, rationale, and semiconductor. A decrease of force and zone should be possible by forfeiting one factor to accomplish the other. In this work, a corner multiplier is planned dependent on a probabilistic methodology. In the truncation part of incomplete items, a probabilistic assessment inclination circuit is presented. Wave Carry Adder (RCA) was supplanted with a conveying Look Ahead (CLA) adder in the execution. Reproductions were done utilizing Synopsys Design Compiler for

saed 90 nm innovation. 9.7% area decrease and 3.9% power decrease were accounted for L = 8 and L = 10 when contrasted and existing work.

Exsisting System

An important function of an arithmetic block is multiplication because, in most mathematical computations, it forms the bulk of the execution time. Thus, the development of a fast multiplier has been a key research area for a long time. Vedic Mathematics is a methodology of arithmetic rules that allows for more efficient implementations regarding speed. Multiplication in this methodology consists of three steps: generation of partial products, reduction of partial products, and finally carry propagate addition. Multiplier design based on Vedic mathematics has many advantages as the partial products and sums are generated in one step, which reduces the carry propagation from LSB to MSB. This feature helps in scaling the design for larger inputs without proportionally increasing the propagation delay as all smaller blocks of the design work concurrently.

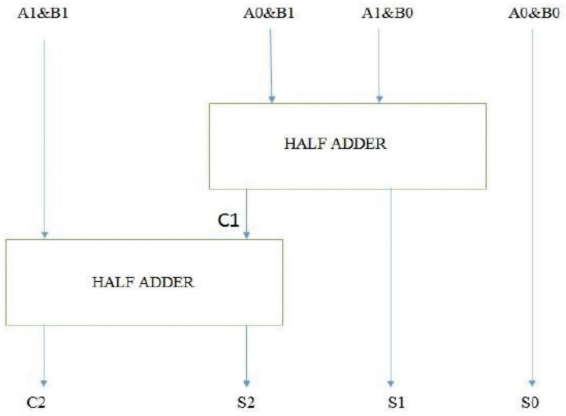
Proposed System

Vedic multiplier plans proposed in the composing rely upon Urdhva Tiryagbhyam and Nikhilam sutras of Vedic Mathematics. As Nikhil sutra is only beneficial for inputs that are close to the power of 10, in this paper an arrangement to perform high-speed increase reliant on the Urdhva Tiryagbhyam sutra of Vedic Mathematics which is a summarized technique for all numbers, has been presented. An arrangement of snake plans has been proposed in the composition to update the introduction of the Vedic multiplier. In this paper, a novel execution of a snake reliant on CSA is proposed, which reduces the pass-on inciting delay in the arrangement by using passing on free math. The proposed snake setup manages a mutt of equal and quaternary number structures wherein the absolute is directly delivered twofold using the possibility of an evolving piece, executing the change module. Vedic-math is an old technique that can be clearly utilized in various pieces of science like polynomial math, calculating, etc. It lessens the multifaceted nature by killing the pointless advances while learning any result. There are 16 sutras in Vedic-math.

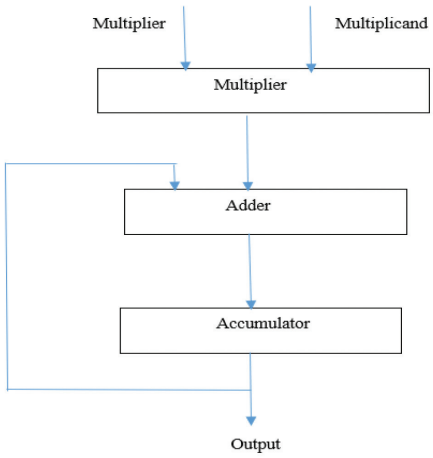
Module Explanation

Among the over 16 sutras, Urdhva Tiryakbhyam (UT) and Nikhilam Navatashcaramam Dashatah (NND) are utilized for processing the duplication of any two numbers. For the most part, the NND sutra is liked for bigger piece numbers and the UT sutra is liked for more modest piece numbers. Thus UT sutra is utilized in this work.

Basic MAC



Implementation of 2 Bit Multiplier



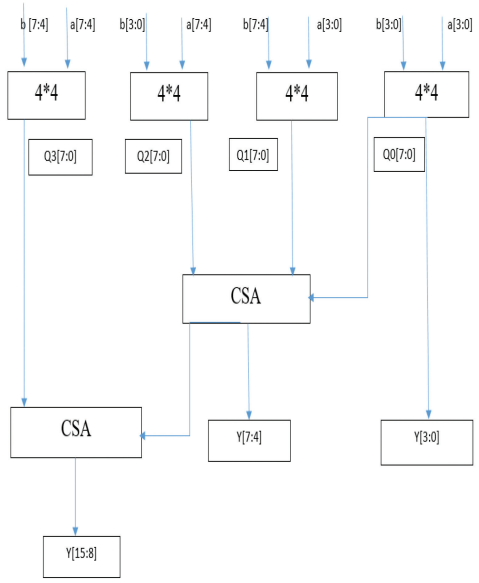
With HA'S

Notwithstanding, the above plan isn't appropriate for higher-request multipliers as it prompts an expansion in delay. Thus, a convey save viper is liked for adding halfway items. Here halfway items are created in an equal way very much like an exhibit multiplier.

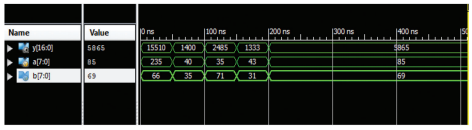
Proposed 8 Bit Multiplier

The 8 bit Vedic-multiplier has been planned by four 4 bit multipliers. Here the data sources a[7:0] and b[7:0] are isolated into a[3:0], a[7:4], b[3:0], b[7:4] separately, and took care of as contributions to the multipliers and an eventual

outcome is a 16-cycle number. Figure 4 addresses the proposed design for the 8 bit multiplier.



OUTPUT



TIMING ANALYSIS (PROPOSED SYSTEM)

```
Data Path: a<2> to y<16>
                              Gate     Net
  Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O            18    1.222    1.154  a_2_IBUF (a_2_IBUF)
   LUT2:I0->O            2    0.203    0.981  vdut1/p91 (vdut1/p9)
   LUT6:I0->O            3    0.203    0.651  vdut1/g26/hcarry1 (vdut1/c3)
   LUT4:I3->O            3    0.205    0.879  vdut1/g27/g191_xo<0>1 (vdut1/w
   LUT6:I3->O            2    0.205    0.961  vdut1/g29/hcarry1 (vdut1/c6)
   LUT6:I1->O            3    0.203    0.879  vdut1/g30/g191_xo<0>1 (vdut1/w
   LUT6:I3->O            3    0.205    0.651  vdut1/g32/hcarry1 (vdut1/c9)
   LUT3:I2->O            2    0.205    0.617  vdut1/g33/g191_xo<0>1 (vdut1/w
   LUT5:I4->O            2    0.205    0.864  vdut1/g34/out1 (vdut1/c11)
   LUT6:I2->O            2    0.203    0.961  vdut1/g35/g191_xo<0>1 (y1<6>)
   LUT6:I1->O            3    0.203    0.995  vdut6/ci<2>1 (vdut6/ci<2>)
   LUT6:I1->O            3    0.203    1.015  vdut6/ci<4>1 (vdut6/ci<4>)
   LUT6:I0->O            3    0.203    0.651  vdut6/ci<6>1 (vdut6/ci<6>)
   LUT4:I3->O            2    0.205    0.961  c1 (c)
   LUT5:I0->O            4    0.203    0.684  vdut8/ci<4>1 (vdut8/ci<4>)
   LUT3:I2->O            1    0.205    0.579  vdut8/Mxor_si<6>_xo<0>1 (y_14_
   OBUF:I->O                  2.571           y_14_OBUF (y<14>)
  ----------------------------------------
  Total                      20.338ns (6.852ns logic, 13.486ns route)
                                      (33.7% logic, 66.3% route)
```

Conclusion

By Comparing both the Existing Vedic multiplier and proposed Vedic multiplier, it is seen that the Proposed Vedic multiplier improves the deferment. Thusly, it is surmised that a multiplier that requires uncommonly fast execution can use such a multiplier in picture and sign taking care of utilizations.

References

[1] Dwivedi, Kavindra & Sharma Sharma, R. K. & Chunduri, Ajay. "**Hybrid Multiplier-Based Optimized MAC Unit**", 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Bangalore, 2018, pp. 1–4.

[2] Jithin, S., Prabhu, E. "**Parallel Multiplier – Accumulator Unit based on Vedic Mathematics**", in ARPN Journal of Engineering and Applied Sciences, Vol. 10, no. 8, pp. 3608–3613, May 2015.

[3] S. N. Gadakh and A. K. Khade. "**Design and Optimization of 16 × 16 Bit Multiplier Using Vedic Mathematics**", in proc. Int. Conf. on Automatic Control and Dynamic Optimization Techniques, 2016.

[4] K. Bathija, R & S. Meena, R & Sarkar, S & Sahu, Rajesh. "**Low Power High Speed 16 × 16 bit Multiplier using Vedic Mathematics**", in International Journal of Computer Applications. 59. 41–44. 10.5120/9556-4016.

[5] M. V. Durga Pavan and Ramesh, S. R. "**An Efficient Booth Multiplier Using Probabilistic Approach**", in 2018 International Conference on Communication and Signal Processing (ICCSP), Chennai, 2018, pp. 365–368.

[6] L. Ranganath, D. Jay Kumar, P. Siva Nagendra Reddy. "**Design of MAC Unit in Artificial Neural Network Architecture using Verilog HDL**", in International conference on Signal Processing, Communication, Power and Embedded System (SCOPES)-2016.

[7] **Carry-Save Addition**. Prof. Loh. CS3220 – Processor Design – Spring 2005.

[8] R. Balakumaran and E. Prabhu. "**Design of high speed multiplier using modified booth algorithm with hybrid carry look-ahead adder**", in 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, 2016, pp. 1–7.

[9] A. Eshack and S. Krishnakumar. "**Implementation of Pipelined Low Power Vedic Multiplier**", in 2nd International Conference on Trends in Electronics and Informatics (ICOEI), Tirunelveli, 2018, pp. 171–174.

[10] S. Rakesh and K. S. V. Grace. "**A survey on the design and performance of various MAC unit architectures**", in 2017 IEEE International Conference on Circuits and Systems (ICCS), Thiruvananthapuram, 2017, pp. 312–315.